UNITED STATES PATENT APPLICATION

FOR

AN INTERFACE DEVICE INCLUDING A VIDEO BIOS COMPONENT

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This Application is a Continuation In Part of commonly assigned, copending U.S.

Application No. 10/197,071, A MULTI-CONFIGURATION GPU INTERFACE

5   DEVICE, by Thomas E. Dewey, et al., which is incorporated herein in its entirety

AN INTERFACE DEVICE INCLUDING A VIDEO BIOS COMPONENT

10   FIELD OF THE INVENTION

The field of the present invention pertains to electronic integrated circuits. More

particularly, the present invention relates to printed circuit board interfaces.

BACKGROUND OF THE INVENTION

15   Computer system manufacturers often employ multiple configurations of

processors, memory, and motherboards. The different configurations are used to satisfy

the different requirements of varying market segments. For example, more powerful

systems can include two or more processors and have provisions for a large amount of

installed RAM. Similarly, more specialized computer systems can include specialized

20   provisions for special function integrated circuit components, such as graphics

accelerators, media processor chips, high-speed input output chips, and the like.

As new configurations of processors, memory, and the like are introduced,

computer system manufacturers need to ensure the correct chip set configuration and

programming information is incorporated into each new system prior to that system being completed and shipped. Failure to correctly match processor and/or memory configuration with chip set programming can lead to faulty operation, or complete failure, of the computer system.

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Configuring chip set programming for computer system graphics processor units (GPUs) can be particularly problematic for computer system manufacturers. GPUs typically have a much greater number of processor type and memory configurations in comparison to the CPU of a computer system. Different versions of a GPU can vary

10 significantly with respect to the capabilities and features implemented. Such variations can include the number and type of integrated circuit dies built within the GPU (e.g., DRAMs, etc.), the type of operations supported by the GPU, and the like. These different versions impact other components which must function with the GPU or CPU. These variations of configuration must be tracked by the computer system manufacturer.

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Consequently, tracking GPU configuration to ensure correct BIOS load out is an important task for computer system manufacturers. GPU configuration tracking information must be maintained and used by the manufacturer to ensure the correct chip set programming information is used with a given GPU configuration. For example,

20 different GPU versions function with video BIOS chips (e.g., mounted on the motherboard) in different manners and support different functions and/or features. Consequently, computer system manufacturers must track what type of GPU goes with what type of motherboard, and in turn, is matched with what version of video BIOS (basic input output system) programming and/or what type of video BIOS chip. This

25 added burden of matching components (e.g., GPU version with video BIOS version) and ensuring the correct programming information is loaded into BIOS ROM imposes an

additional cost on system manufacturers, and is a significant source of error and unreliability.

Thus what is required is a device that can ensure the correct version of BIOS programming is loaded with a given GPU configuration. What is required is an interface device that eliminates the burden of matching components with different processor versions.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide an interface device including a video BIOS component. Embodiments of the present invention enable the programming of the video BIOS component in accordance with a specific GPU version prior to GPU installation on a motherboard. Additionally, embodiments of the present invention match video BIOS components with specific GPU versions while maintaining a standardized interface for coupling to a printed circuit board.

In one embodiment, the present invention is implemented as an interface device having a video BIOS component. The device includes a substrate for implementing a mother board connection and implementing a GPU (graphics processor unit) connection. A video BIOS component is mounted on the substrate for providing video BIOS functions for the computer system. This aspect allows the video BIOS component to be programmed, for example, by the GPU manufacturer, prior to the build out of a computer system by a board assembler, thereby eliminating any need for the board assembler to track GPU versions in order to program video BIOS components in accordance with specific GPU versions.

In one embodiment, the substrate of the interface device is configured to support a wire bonded attachment to a GPU and the video BIOS component. In another embodiment, a plurality of memory components (e.g., DRAMs chips) are mounted on the substrate with the video BIOS component and a GPU. Additionally, the substrate can support a flip chip mounted GPU.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of

limitation, in the figures of the accompanying drawings and in which like reference

numerals refer to similar elements and in which:

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Figure 1 shows a GPU interface system in accordance with one embodiment of the

present invention.

Figure 2 shows a top-down view of the interface device in accordance with one

10   embodiment of the present invention.

Figure 3 shows a first configuration and a second configuration of a GPU package

device in accordance with one embodiment of the present invention.

15   Figure 4 shows an example of a computer system in accordance with one

embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be

5   understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of embodiments of the present invention, numerous specific details are set forth in order to

10   provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the embodiments of the present invention.

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Embodiments of the present invention provide an interface device including a video BIOS component. Embodiments of the present invention enable the programming of the video BIOS component in accordance with a specific GPU version prior to GPU installation on a motherboard. Additionally, embodiments of the present invention match

20   video BIOS components with specific GPU versions while maintaining a standardized interface for coupling to a printed circuit board. Embodiments of the present invention and their benefits are further described below.

Notation and Nomenclature

Some portions of the detailed descriptions which follow are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and

5 representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, computer executed step, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not

10 necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

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It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions

20 utilizing terms such as "providing" or "programing" or "processing" or the like, refer to the action and processes of a computer system (e.g., computer system 400 of Figure 4), or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories

into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Figure 1 shows a GPU interface system 100 in accordance with one embodiment of the present invention. As depicted in Figure 1, system 100 shows a plurality of different types of GPUs 101 using an interface device 102 to couple to a PCB 103.

In the system 100 embodiment, the interface device 102 functions as a multi-configuration interface device for coupling different types of GPUs to a PCB (printed circuit board). The interface device 102 comprises a GPU interface 105 for a connection to the GPUs 101 and a PCB interface 160 for a connection to the PCB 103.

In this embodiment, the GPU interface 105 is implemented using a customizable attachment footprint 109 for effectuating a connection to differing GPU types 101 while maintaining the PCB interface 160 for the connection to the PCB 103. In accordance with the requirements of a GPU type, the customizable attachment footprint can include a solder ball array, an array of contact pads, or the like, arranged in a fashion to support the attachment of the GPU type. The attachment footprint 109 for different GPUs 101 can be configured (e.g., during manufacturing) to respectively support them (e.g., different ball counts, interface configurations, power-ground connections, contact pad geometry, and the like). The interface device 102 maintains a consistent PCB interface 160. Thus, as the characteristics of the different types of GPUs 101 change and evolve, or as different GPU versions 101 are implemented, a consistent connection can be maintained for the

PCB via the PCB interface 160. Differing GPU types can be, for example, different types of graphics processor integrated circuits, identical graphics processor integrated circuits and differing amounts of memory, or the like.

5   Additionally, the interface device embodiments utilize compact and inexpensive attachment footprints (e.g., ball grid arrays, contact pads, etc.) to implement the GPU connection as opposed to prior art socket and slot interconnections. For example, ball grid arrays are more flexible than prior art slot connections or socket connections. For example, the customizable attachment footprint 109 of the present embodiment can

10   accept a surface mounted GPU, substrate mounted GPU, and the like, as described below.

Figure 2 shows a top-down view of the interface device 102 in accordance with one embodiment of the present invention. As depicted in Figure 2, the interface device 102 includes the GPU interface 105 having the customizable attachment footprint 109

15   (e.g., not drawn to scale).

In accordance with differing requirements of different GPU types, the GPU interface 105 is configured to support different means of attachment for a given GPU type. For example, in one embodiment, the GPU interface 105 is configured to support a

20   wire bond attachment to a GPU. In another embodiment, the GPU interface 105 is configured to support a substrate, wherein the substrate includes a mounted GPU in either a surface mounted configuration or a flip chip mounted configuration. In another embodiment, the GPU interface 105 can include a nonfunctional area 111 centrally

disposed within the GPU interface 105 to implement either a solder attachment to a surface of a GPU (e.g., a flip chip mounted GPU on a substrate or on the device) or an adhesive attachment.

5   In a substrate mounted GPU embodiment, the customizable attachment footprint 109 of the GPU interface 105 can be configured to support a plurality of different RAM component configurations (e.g., one, two, four RAM components, etc.) mounted on the substrate in addition to the GPU (e.g., including an additional number of power and ground balls to support the RAM components, voltage reference balls for the RAM

10   components, and the like).

Referring still to Figure 2, in the present embodiment, the customizable attachment footprint 109 includes a first area located at the center of the customizable attachment footprint 109 (e.g., the balls immediately surrounding the nonfunctional area

15   111) and a second area disposed around the periphery of the centrally located first area. The balls of the first area include a plurality of thermal balls to support a wire bond attachment to a GPU. The customizable attachment footprint 109 includes a number of ground assignment balls in the signal ball rows (outer 7 rows of the array). The thermal balls in the center area (e.g., the balls immediately surrounding the nonfunctional area 111)

20   are used for the wire-bond versions. Additionally, the ground to signal ratio among the balls of the customizable attachment footprint 109 is also relatively high, in comparison to prior art, thereby providing improved return paths for high speed signaling. The added number of peripheral ground balls provide a significant advantage to designs where the

thermal ground balls in the center of the array (e.g., in the first area) provide both signal interconnections and function as the means of electrical grounding and return paths.

The customizable attachment footprint 109 supports separate power and ground
5   balls for memory and core power. In one embodiment, these balls are primarily disposed in the corners of the customizable attachment footprint 109. In a case where the interface device 102 supports a substrate mounted GPU, this aspect permits the substrate to mount a number of memory components in addition to the GPU (e.g., two or more RAM memory components).

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Embodiments of the customizable attachment footprint 109 have sufficient power, ground, and impedance calibration ball assignments to support different versions of the industry standard AGP (accelerated graphics port) interface. For example, the customizable attachment footprint 109 can be configured to support AGP 2x, AGP 4x, or
15   AGP 8x compatible GPUs. Thus, for example, the interface device 102 can readily support a majority of the GPUs being manufactured to function with AGP 4x, and be easily configured to support AGP 8x, or greater, GPU designs when they arrive.

Embodiments of the customizable attachment footprint 109 support ball
20   assignments for the different versions of AGP as described above. Additionally, the customizable attachment footprint 109 can be configured to support dual DACs (to support dual display monitors), digital-video-out (to support digital LCD displays, etc.), TMDS (temperature minimized differential signaling), LVDS (low voltage differential

signaling), VIP (video interface port), memory interface (e.g., ROM), and general purpose

IOs. Thus, each customizable attachment footprint 109 implementation can be

configured to support a number of different subsets of this super-set of GPU interfaces.

This allows designers to trade differing degrees of functionality with differing costs and

5   price points.

Additionally, embodiments of the customizable attachment footprint 109 include

balls assigned for external frame-buffer clock termination and frame-buffer VREF circuits.

Each customizable attachment footprint 109 implementation can choose to connect to

10   these external circuits or not.

It should be noted that although embodiments of the present invention have been

discussed in terms a GPU and a GPU interface, embodiments of the present invention are

also well-suited to use with a general purpose CPU and CPU interface.

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Figure 3 shows a first configuration and a second configuration of a GPU package

device in accordance with one embodiment of the present invention. As shown in Figure

3, a first configuration of the device, configuration A, includes a processor (e.g., GPU)

130 and a plurality of memory components 121-124 mounted on a substrate 110. A

20   second configuration, configuration B, includes a processor 150 and a plurality of memory

components 141-142 mounted on a substrate 120. Configuration A and configuration B

are both designed to mount on a common PCB interface 160.

In accordance with embodiments of the present invention, configuration A and configuration B both include respective video BIOS components 131-151. Both devices (e.g., device 110 and device 120) depicted in Figure 3 are implemented as a GPU package device having a GPU and a video BIOS component. The GPU packages include a GPU

5   (e.g., processor 130 and processor 150 respectively) for providing graphics processing for a computer system, in this embodiment, through the common PCB interface 160. Each GPU package itself has an interface for coupling to the common PCB interface 160. Electronic signals from a GPU package communicate with the motherboard of the computer system through the common PCB interface 160. The GPU packages also

10   include a video BIOS component (e.g., a video BIOS chip) for interfacing with the GPU and providing video BIOS functions for the computer system.

Embodiments of the present invention match the video BIOS component with the specific GPU version. Thus, for example, the video BIOS component 131 is programmed

15   specifically in accordance with the components and the configuration (e.g., configuration A) of device 110. Similarly, the video BIOS component 151 is programmed specifically in accordance with the components and configuration (e.g., Configuration B) of device 120. This aspect provides a significant benefit where video BIOS components are matched during manufacture of the GPU package with specific GPU versions. For

20   example, during manufacture, the video BIOS component 131 is recognized, programmed, and included with configuration A while the video BIOS component 151 is recognized, programmed, and included with configuration B. This relieves a computer system manufacturer of the responsibility of tracking which configuration of a graphics package

(e.g., GPU package) goes with what configuration of video BIOS component. Additionally, this benefit is provided while maintaining a standardized interface for coupling to a printed circuit board (e.g., through common PCB interface 160).

5   Referring still Figure 3, as described above, embodiments of the present invention are well-suited for use with an interface device comprising a configurable substrate that is adapted to support multiple combinations and mounting configurations of processors (e.g., GPUs, DSPs, CPUs, etc.) and memory components (e.g., DDR DRAMs, etc.) while still maintaining a common interface to, for example, an interface area of a printed

10   circuit board (e.g., motherboard, etc.). For example, an interface device comprising the configurable substrate with a mounted video BIOS component can be manufactured such that the interface device will subsequently support many different combinations of GPUs, memory components, and the like, thereby allowing, for example, a GPU manufacter to build multiple configurations of preprogrammed GPU packages using a

15   common interface device. Each of these multiple GPU package types can have their respective video BIOS programmed by the GPU manufacturer as opposed to forcing the GPU version tracking, verification, and programming process on, for example, a board assembler.

20   As shown in Figure 3, configuration A has four memory components 121-124, a video BIOS component 131, and a single processor 130. Configuration B has 2 memory components 141-142, a video BIOS component 151, and a single processor 150. Both configurations utilize a common substrate interface that is designed to couple to the

common PCB interface 160. It should be noted that embodiments can be configured to support other combinations of memory components and processor (e.g., one processor and one memory component, eight memory components, 16 memory components, etc.).

5   In one embodiment, the memory components 121-124 and 141-142, and the video BIOS components 131-151 are prepackaged integrated circuit components. As used herein, prepackaged integrated circuit components refer to memory components and video BIOS components that are not bare dies, or raw chips. The components are packaged in the conventional fashion and are tested prior to being mounted on the substrate 110 or the

10   substrate 120. The use of prepackaged pre-tested components increases the yield of the overall device fabrication process in comparison to prior art MCM (multichip module) or MCP (multichip package) devices, which utilize raw chips. Additionally, the use of prepackaged components simplifies their acquisition process. For example: prepackaged components can be purchased from a greater number of vendors, providing better

15   flexibility with respect to price and/or quality.

        In the configuration A and configuration B embodiments shown in Figure 3, the memory components and the video BIOS components are surface mounted on the substrate 110 or 120. In configuration B, the processor 150 is surface mounted on the

20   substrate 120 along with the memory/via BIOS components. In configuration A, the processor 130 is mounted on the substrate 110 in a flip-chip configuration, on the underside of the substrate 110, as shown by the dotted lines showing the outline of the processor 130.

In one embodiment, the processors 130 and 140 are GPUs (graphics processor units). In other embodiments, the processors 130 and 140 are other types of processors, such as, for example, DSPs (digital signal processors), CPUs (central processing units), or

5   the like. Similarly, in one embodiment, the memory components 121-124 and 141-142 are DDR memory components. In other embodiments, the memory components 121-124 and 141-142 are other types of memory components, such as, for example, RDRAM memory components, SDRAM memory components, or the like. In one embodiment, the video BIOS components 131-151 are flash ROMs.

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Computer System Platform

With reference now to Figure 4, a computer system 400 in accordance with one embodiment of the present invention is shown. Computer system 400 shows the components of a computer system in accordance with one embodiment of the present

15   invention that provides the execution platform for implementing certain software-based functionality of the present invention. As described above, certain processes and steps of the present invention are realized, in one embodiment, as a series of instructions (e.g., software program) that reside within computer readable memory units of a computer system (e.g., system 400) and are executed by the CPU of system 400. When executed,

20   the instructions cause the computer system 400 to implement the functionality of the present invention as described below.

In general, computer system 400 comprises at least one CPU 401 coupled to a system memory 415 and a graphics package 410 via one or more busses as shown. The graphics package 410 is coupled to a display 412. The graphics package 410 includes a GPU 416 for providing graphics processing functions and a video BIOS component 417

5   for providing video BIOS functions. As shown in Figure 4, system 400 shows the basic components of a computer system platform that implements the functionality of the present invention. Accordingly, system 400 can be implemented as, for example, a desktop computer system or server computer system, having a powerful general-purpose CPU 401 coupled to a dedicated graphics rendering graphics package 410. In such an

10   embodiment, components would be included that are designed to add peripheral buses, specialized graphics memory and system memory, IO devices, and the like. Additionally, it should be appreciated that although the graphics package 410 is depicted in Figure 4 as a discrete component, the graphics package 410 can be implemented as a discrete graphics card designed to couple to the computer system via a graphics port (e.g., AGP port, or

15   the like), as a discrete integrated circuit die (e.g., mounted directly on the motherboard), or as an integrated GPU included within the integrated circuit die of a computer system chipset (e.g., integrated within the Northbridge chip). Similarly, system 400 can be implemented as a set-top video game console device such as, for example, the Xbox®, available from Microsoft Corporation of Redmond, Washington.

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The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many

modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the

5   particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.